In the Abstract:

Please amend the Abstract as follows:

All Pointer-based accesses require first that the value contained in a pointer register ~~(200a, 200b, 200c, 200d)~~ to be read and then that value be used as an address to the appropriate region in random access memory (RAM) ~~(104)~~. As implemented today, this requires two memory read access cycles, each of which takes at least one clock cycle and therefore this implementation does not allow single cycle operation. In accordance with an embodiment of the invention, when an access is performed to pointer memory ~~(103a, 103b, 103c, 103d)~~ to read the contents of a pointer, it is the shadow memory that is actually read and that returns the pointer value. Since the shadow memory is made up of pointer registers ~~(200a, 200b, 200c, 200d)~~, a read access involves mutliplexing out of appropriate data for the pointer address from these pointer registers ~~(200a, 200b, 200c, 200d)~~ to form a target pointer address. This target pointer address is then used as an address to access RAM ~~(104)~~ without the overhead of a clock, since the register access is purely combinatorial and does not require clock-phase related timing as does access to the RAM ~~(104)~~.